ABSTRACT

A new test data compression method and decompression apparatus is invented for SoC (System-on-a-Chip) architecture. The method is based on analyzing the factors that influence test parameters: compression ratio and hardware overhead. To improve compression ratio, the proposed method is based on Modified Statistical Coding (MSC) and input reduction (IR) scheme, as well as a novel mapping and re-ordering algorithm proposed in a preprocessing step. Unlike previous approaches using the CSR architecture, the inventive method is to compress original test data, but not T_{diff}, and decompress the compressed test data without the CSR architecture. Therefore, the proposed method leads to better compression ratio with lower hardware overhead than previous works. An experimental comparison on ISCAS '89 benchmark circuits validates the proposed method.